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Robert E. Krebs, Esq.
THELEN REID & PRIEST LLP
P.O. Box 640640
SANJOSE, CA 95164-0640

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PATHAK, SUDHANSHU C

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2634

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Please find below and/or attached an Office communication concerning this application or proceeding.

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| Office Action Summary | Application No. 09/802,544 | Applicant(s) POURSEYED ET AL. | |
| | Examiner Sudhanshu C. Pathak | Art Unit 2634 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on September 27th, 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on March 9th, 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-to-33 are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7 & 9-33 are rejected under 35 U.S.C. 102(b) as being anticipated by the Applicant Admitted Prior Art (AAPA).

Regarding to Claims 1 & 12, the Applicant Admitted Prior Art (AAPA) discloses a system and method for demodulating narrowband signals from a received signal (Fig. 1, elements 10, 28) comprising a downconverter operative to downconvert the received signal (Fig. 1, elements 16-52); and a baseband processor in electrical communication with the downconverter, the baseband processor being operative to decode the narrowband signal from the received signal (Fig. 1, element 54).

Regarding to Claims 2 & 15, the AAPA discloses a system and method for demodulating narrowband signals from a received signal comprising a downconverter and a baseband processor as described above. The AAPA further discloses the downconverter comprising at least one analog-to-digital converter (ADC) operative to convert the received signal to a digital signal (Fig. 1, elements 42 a/b & 52 a/b).

Regarding to Claim 3, the AAPA discloses a system for receiving and demodulating narrowband signals from a received signal comprising a downconverter and a baseband processor, wherein the downconverter further comprising at least one analog-to-digital converter (ADC), as described above. The AAPA further discloses the downconverter comprising at least one demodulator (Fig. 1, elements 34, 46).

Regarding to Claims 4, 16 & 27, the AAPA discloses a system and method for demodulating narrowband signals from a received signal comprising a downconverter and a baseband processor to decode the received digital signal, wherein the downconverter further comprising at least one analog-to-digital converter (ADC) and at least one demodulator, as described above. The AAPA further discloses the demodulator is a quadrature demodulator operative to demodulate the received signal, prior to converting the signal to a digital signal, into two signals shifted in phase (Fig. 1, elements 34, 46, 38a/b & Specification, Page 8, lines 3-18).

Regarding to Claims 5 & 17, the AAPA discloses a system and method for demodulating narrowband signals from a received signal comprising a downconverter and a baseband processor, wherein the downconverter further comprising at least one analog-to-digital converter (ADC) and at least one demodulator, wherein the demodulator further is a quadrature demodulator, as described above. The AAPA further discloses the downconverter comprising a mixer operative to mix the received signal prior to demodulation (Fig. 1, element 20).

Regarding to Claims 6 & 18, the AAPA discloses a system and method for demodulating narrowband signals from a received signal comprising a downconverter and a baseband processor, wherein the downconverter further comprising at least one analog-to-digital converter (ADC), at least one demodulator and a mixer, wherein the demodulator further is a quadrature demodulator, as described above. The AAPA further discloses the downconverter comprising an amplifier operative to increase the gain (amplifying) of the received signal prior to demodulation (Fig. 1, element 16).

Regarding to Claims 7 & 19, the AAPA discloses a system and method for demodulating narrowband signals from a received signal comprising a downconverter and a baseband processor as described above. The AAPA further discloses the system comprising an antenna in electrical communication with the downconverter and operative to detect the received signal (Fig. 1, element 12).

Regarding to Claim 9, the AAPA discloses a system for demodulating narrowband signals from a received signal comprising a downconverter and a baseband processor as described above. The AAPA further discloses the baseband processor is operative to decode a narrowband signal having a bandwidth of 30kHz (Fig. 1, elements 28, 54 & Specification, Page 7, lines 3-5, 15-21).

Regarding to Claims 10, 13 & 28-32, the AAPA discloses a system and method for demodulating narrowband signals from a received signal comprising a downconverter, further comprising an ADC and a demodulator, and a baseband processor as described above. The AAPA further discloses the baseband processor

is operative to decode wideband signals as well as narrowband signals (Fig. 1, elements 26, 28, 54 & Specification, Page 7, lines 15-21).

Regarding to Claims 11, 14 & 33, the AAPA discloses a system and method for demodulating narrowband and wideband signals from a received signal comprising a downconverter and a baseband processor as described above. The AAPA further discloses the baseband processor is operative to decode a narrowband signal having a bandwidth of 30kHz and the wideband signals have a bandwidth of 200kHz (Fig. 1, elements 26, 28, 54 & Specification, Page 7, lines 3-5, 15-21).

Regarding to Claims 20 & 21, the AAPA discloses a wireless wideband receiver operative to receive at least one 200kHz (wideband) channel (Fig. 1, elements 10, 26 & Specification, Page 6, lines 20-24 – to – Page 7, lines 1-25), the receiver comprising an antenna operative to detect a received signal (Fig. 1, element 12); a switch filter in electrical communication with the antenna, the switch filter being operative to switch between the received signal and a transmitted signal (Fig. 1, element 14); an amplifier in electrical communication with the switch filter, the amplifier being operative to increase the gain of the received signal (Fig. 1, element 16); a mixer in electrical communication with the amplifier, the mixer being operative to mix the received signal with a radio frequency oscillation signal (Fig. 1, element 20); a demodulator in electrical communication with the mixer, the demodulator being operative to demodulate the received signal with an intermediate frequency oscillation signal (Fig. 1, elements 34, 36); an analog to digital converter in electrical communication with the demodulator, the analog to digital converter being operative

to convert the received signal to a digital signal (Fig. 1, elements 42 a/b); and a baseband processor in electrical communication with the analog to digital converter, the baseband processor being configured to decode the narrowband and wideband channel from the received signal (Fig. 1, elements 26, 28, 54).

Regarding to Claim 22, the AAPA discloses a wireless wideband receiver comprising an antenna, a switch filter, an amplifier, a mixer, a demodulator, an analog-to-digital converter (ADC), and a baseband processor configured to decode a narrowband and wideband received signal as described above. The AAPA further discloses the receiver comprising a radio frequency phase lock loop (RF PLL) in electrical communication with the mixer, the RF PLL being operative to generate the radio frequency oscillation signal (Fig. 1, element 22).

Regarding to Claim 23, the AAPA discloses a wireless wideband receiver comprising an antenna, a switch filter, an amplifier, a mixer, a demodulator, an analog-to-digital converter (ADC), a baseband processor configured to decode a narrowband and wideband received signal, and a RF PLL as described above. The AAPA further discloses the receiver comprising an intermediate frequency phase lock loop (IF PLL) in electrical communication with the demodulator, the IF PLL being operative to generate the intermediate frequency oscillation signal (Fig. 1, element 36).

Regarding to Claim 24, the AAPA discloses a wireless wideband receiver comprising an antenna, a switch filter, an amplifier, a mixer, a demodulator, an analog-to-digital converter (ADC), a baseband processor configured to decode a

narrowband and wideband received signal, a RF PLL and an IF PLL as described above. The AAPA further discloses the demodulator is a quadrature demodulator operative to demodulate the received signal into two demodulated signals having quadrature phase (Fig. 1, elements 34, 46, 38a/b & Specification, Page 8, lines 3-18).

Regarding to Claim 25, the AAPA discloses a wireless wideband receiver comprising an antenna, a switch filter, an amplifier, a mixer, a quadrature demodulator, an analog-to-digital converter (ADC), a baseband processor configured to decode a narrowband and wideband received signal, a RF PLL and an IF PLL as described above. The AAPA further discloses the ADC comprising two ADC's operative to convert the two received signals to digital signals (Fig. 1, elements 42 a/b, 52 a/b).

Regarding to Claim 26, the AAPA discloses a wireless wideband receiver comprising an antenna, a switch filter, an amplifier, a mixer, a quadrature demodulator, an analog-to-digital converter (ADC), wherein the ADC further comprises two ADC's, a baseband processor configured to decode a narrowband and wideband received signal, a RF PLL and an IF PLL as described above. The AAPA further discloses the narrowband channel having a bandwidth of 30kHz and the wideband channel have a bandwidth of 200kHz (Fig. 1, elements 26, 28, 54 & Specification, Page 7, lines 3-5, 15-21).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art (AAPA) in view of Lucidarme et al. (6,704,546).

Regarding to Claims 1, 12 & 8, The Applicant Admitted Prior Art (AAPA) discloses a system for downconverting a received signal having a wideband and narrowband signal components (Fig. 1) the system comprising a downconverter components (Fig. 1, elements 16-52) to downconvert the received signal for baseband processing, and a baseband processor, for baseband processing, in electrical communication with the downconverter, the baseband processor being operative to decode the narrowband signal from the received signal (Fig. 1, element 54). However, the AAPA does not disclose a single down converter path (components) operative to downconvert both the wideband and narrowband signal components of the received signal.

Lucidarme discloses a method and apparatus for transmitting and receiving wideband and narrowband signals in various different radio telecommunications systems (Column 1, lines 5-49, 60-67 & Column 2, lines 1-25 & Column 7, lines 58-67 & Column 12, lines 60-61 & Fig. 2a-2b, elements "W", "N" & Fig.'s 6-7).

Lucidarme further discloses a single downconverter path for receiving and

downconverting both the wideband and narrowband signals (Fig. 7, elements 459, 458, 462, 463 & Column 9, lines 45-58). Lucidarme also discloses a variable digital filter for varying the bandwidth of the received signal depending on the received channels depending on the protocol (Fig. 7, elements 465, 466, 467 & Column 10, lines 1-60). Lucidarme also discloses a frequency allocation manager (FAM) for the allocation of a frequency band and the variable digital filter, implemented in a programmable processor, configured to filter a received signal into a wideband and narrowband channels, by varying the bandwidth of the variable digital filter bandwidth (Fig.'s 5-to-7 & Abstract, lines 1-15 & Column 1, lines 5-17, 40-67 & Column 2, lines 1-25 & Column 3, lines 60-67 & Column 4, lines 1-15 & Column 6, lines 19-38, 52-60 & Column 7, lines 23-67 & Column 8, lines 1-67 & Column 9, lines 1-58 & Column 10, lines 1-50 & Column 12, lines 60-65 & Column 15, lines 41-67 & Column 16, lines 63-67 & Column 17, lines 1-2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Lucidarme teaches implementing a single downconverter path and the selection of the narrowband or wideband signals in the processor with the FAM and the variable digital filter, and this can be implemented in the apparatus as described in the AAPA so as to reduce the analog components for downconversion and implement the transceiver in multiple protocols (and applications) requiring various different channel bandwidths and center frequencies.

Regarding to Claims 2 & 15, the AAPA in view of Lucidarme discloses a system for downconverting a received signal having a wideband and narrowband signal

components comprising a single downconverter path and a baseband processor in electrical communication with the downconverter being operative to demodulate and decode the narrowband signal from the downconverted received signal as described above. The AAPA further discloses the downconverter comprising at least one analog-to-digital converter (ADC) operative to convert the received signal to a digital signal (Fig. 1, elements 42 a/b & 52 a/b). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Lucidarme teaches implementing a single downconverter path and the selection of the narrowband or wideband signals in the processor with the FAM and the variable digital filter, and this can be implemented in the apparatus as described in the AAPA so as to reduce the analog components for downconversion and implement the transceiver in multiple protocols (and applications) requiring various different channel bandwidths and center frequencies, thus satisfying the limitation of the claim.

Regarding to Claim 3, the AAPA in view of Lucidarme discloses a system for downconverting a received signal having a wideband and narrowband signal components comprising a single downconverter path and a baseband processor in electrical communication with the downconverter being operative to demodulate and decode the narrowband signal from the downconverted received signal, wherein the downconverter further comprising at least one analog-to-digital converter (ADC), as described above. The AAPA further discloses the downconverter comprising a demodulator operative to demodulate the received signal into two phase shifted signals (Fig. 1, element 46). Therefore, it would have been obvious to one of

ordinary skill in the art at the time of the invention that Lucidarme teaches implementing a single downconverter path and the selection of the narrowband or wideband signals in the processor with the FAM and the variable digital filter, and this can be implemented in the apparatus as described in the AAPA so as to reduce the analog components for downconversion and implement the transceiver in multiple protocols (and applications) requiring various different channel bandwidths and center frequencies, thus only a single demodulator would be required for the downconverter, and duplicate analog components for the wideband and narrowband components would not be required.

Regarding to Claims 4, 16 & 27, the AAPA in view of Lucidarme discloses a system for downconverting a received signal having a wideband and narrowband signal components comprising a single downconverter path and a baseband processor in electrical communication with the downconverter being operative to demodulate and decode the narrowband signal from the downconverted received signal, wherein the downconverter further comprising at least one analog-to-digital converter (ADC) and a single demodulator, as described above. The AAPA further discloses the demodulator is a quadrature demodulator operative to demodulate the received signal, prior to converting the signal to a digital signal, into two signals shifted in phase (Fig. 1, elements 34, 46, 38a/b & Specification, Page 8, lines 3-18). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Lucidarme satisfies the limitations of the claim.

Regarding to Claims 5 & 17, the AAPA in view of Lucidarme discloses a system for downconverting a received signal having a wideband and narrowband signal components comprising a single downconverter path and a baseband processor in electrical communication with the downconverter being operative to demodulate and decode the narrowband signal from the downconverted received signal, wherein the downconverter further comprising at least one analog-to-digital converter (ADC) and a single demodulator, wherein the demodulator further is a quadrature demodulator, as described above. The AAPA further discloses the downconverter comprising a mixer operative to mix the received signal prior to demodulation (Fig. 1, element 20). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Lucidarme satisfies the limitations of the claim.

Regarding to Claims 6 & 18, the AAPA in view of Lucidarme discloses a system for downconverting a received signal having a wideband and narrowband signal components comprising a single downconverter path and a baseband processor in electrical communication with the downconverter being operative to demodulate and decode the narrowband signal from the downconverted received signal, wherein the downconverter further comprising at least one analog-to-digital converter (ADC), a single demodulator and a mixer, wherein the demodulator further is a quadrature demodulator, as described above. The AAPA further discloses the downconverter comprising an amplifier operative to increase the gain (amplifying) of the received signal prior to demodulation (Fig. 1, element 16). Therefore, it would have been

obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Lucidarme satisfies the limitations of the claim.

Regarding to Claims 7 & 19, the AAPA in view of Lucidarme discloses a system for downconverting a received signal having a wideband and narrowband signal components comprising a single downconverter path and a baseband processor in electrical communication with the downconverter being operative to demodulate and decode the narrowband signal from the downconverted received signal as described above. The AAPA further discloses the system comprising an antenna in electrical communication with the downconverter and operative to detect the received signal (Fig. 1, element 12). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Lucidarme satisfies the limitations of the claim.

Regarding to Claim 9, the AAPA in view of Lucidarme discloses a system for downconverting a received signal having a wideband and narrowband signal components comprising a single downconverter path and a baseband processor in electrical communication with the downconverter being operative to demodulate and decode the narrowband signal from the downconverted received signal as described above. The AAPA further discloses the baseband processor is operative to decode a narrowband signal having a bandwidth of 30kHz (Fig. 1, elements 28, 54 & Specification, Page 7, lines 3-5, 15-21). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Lucidarme satisfies the limitations of the claim.

Regarding to Claims 10, 13 & 28-32, the AAPA in view of Lucidarme discloses a system for downconverting a received signal having a wideband and narrowband signal components comprising a single downconverter path and a baseband processor in electrical communication with the downconverter being operative to demodulate and decode the narrowband signal from the downconverted received signal, further comprising an ADC and a demodulator, and a baseband processor as described above. The AAPA further discloses the baseband processor is operative to decode wideband signals as well as narrowband signals (Fig. 1, elements 26, 28, 54 & Specification, Page 7, lines 15-21). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Lucidarme satisfies the limitations of the claim.

Regarding to Claims 11, 14 & 33, the AAPA in view of Lucidarme discloses a system for downconverting a received signal having a wideband and narrowband signal components comprising a single downconverter path and a baseband processor in electrical communication with the downconverter being operative to demodulate and decode the narrowband and wideband signals from the downconverted received signal, further comprising an ADC and a demodulator, and a baseband processor as described above. The AAPA further discloses the baseband processor is operative to decode a narrowband signal having a bandwidth of 30kHz and the wideband signals have a bandwidth of 200kHz (Fig. 1, elements 26, 28, 54 & Specification, Page 7, lines 3-5, 15-21). Therefore, it would have been

obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Lucidarme satisfies the limitations of the claim.

Regarding to Claims 20 & 21, the AAPA discloses a wireless wideband receiver operative to receive at least one 200kHz (wideband) channel (Fig. 1, elements 10, 26 & Specification, Page 6, lines 20-24 – to – Page 7, lines 1-25), the receiver comprising an antenna operative to detect a received signal (Fig. 1, element 12); a switch filter in electrical communication with the antenna, the switch filter being operative to switch between the received signal and a transmitted signal (Fig. 1, element 14); an amplifier in electrical communication with the switch filter, the amplifier being operative to increase the gain of the received signal (Fig. 1, element 16); a mixer in electrical communication with the amplifier, the mixer being operative to mix the received signal with a radio frequency oscillation signal (Fig. 1, element 20); a demodulator in electrical communication with the mixer, the demodulator being operative to demodulate the received signal with an intermediate frequency oscillation signal (Fig. 1, elements 34, 36); an analog to digital converter in electrical communication with the demodulator, the analog to digital converter being operative to convert the received signal to a digital signal (Fig. 1, elements 42 a/b); and a baseband processor in electrical communication with the analog to digital converter, the baseband processor being configured to decode the narrowband and wideband channel from the received signal (Fig. 1, elements 26, 28, 54). However, the AAPA does not disclose a single down converter path (components) operative to

downconvert both the wideband and narrowband signal components of the received signal further comprising a single demodulator.

Lucidarme discloses a method and apparatus for transmitting and receiving wideband and narrowband signals in various different radio telecommunications systems (Column 1, lines 5-49, 60-67 & Column 2, lines 1-25 & Column 7, lines 58-67 & Column 12, lines 60-61 & Fig. 2a-2b, elements "W", "N" & Fig.'s 6-7).

Lucidarme further discloses a single downconverter path for receiving and downconverting both the wideband and narrowband signals (Fig. 7, elements 459, 458, 462, 463 & Column 9, lines 45-58). Lucidarme also discloses a variable digital filter for varying the bandwidth of the received signal depending on the received channels depending on the protocol (Fig. 7, elements 465, 466, 467 & Column 10, lines 1-60). Lucidarme also discloses a frequency allocation manager (FAM) for the allocation of a frequency band and the variable digital filter, implemented in a programmable processor, configured to filter a received signal into a wideband and narrowband channels, by varying the bandwidth of the variable digital filter bandwidth (Fig.'s 5-to-7 & Abstract, lines 1-15 & Column 1, lines 5-17, 40-67 & Column 2, lines 1-25 & Column 3, lines 60-67 & Column 4, lines 1-15 & Column 6, lines 19-38, 52-60 & Column 7, lines 23-67 & Column 8, lines 1-67 & Column 9, lines 1-58 & Column 10, lines 1-50 & Column 12, lines 60-65 & Column 15, lines 41-67 & Column 16, lines 63-67 & Column 17, lines 1-2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Lucidarme teaches implementing a single downconverter path and the selection of the

narrowband or wideband signals in the processor with the FAM and the variable digital filter, and this can be implemented in the apparatus as described in the AAPA so as to reduce the analog components for downconversion and implement the transceiver in multiple protocols (and applications) requiring various different channel bandwidths and center frequencies, thus only a single demodulator would be required for the downconverter, and duplicate analog components for the wideband and narrowband components would not be required.

Regarding to Claim 22, the AAPA in view of Lucidarme discloses a wireless wideband receiver for downconverting a received signal having a wideband and narrowband signal components comprising a single downconverter path and a baseband processor in electrical communication with the downconverter being operative to demodulate and decode the narrowband signal from the downconverted received signal comprising an antenna, a switch filter, an amplifier, a mixer, a demodulator, an analog-to-digital converter (ADC), and a baseband processor configured to decode a narrowband and wideband received signal as described above. The AAPA further discloses the receiver comprising a radio frequency phase lock loop (RF PLL) in electrical communication with the mixer, the RF PLL being operative to generate the radio frequency oscillation signal (Fig. 1, element 22). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Lucidarme satisfies the limitations of the claim.

Regarding to Claim 23, the AAPA in view of Lucidarme discloses a wireless wideband receiver for downconverting a received signal having a wideband and narrowband signal components comprising a single downconverter path and a baseband processor in electrical communication with the downconverter being operative to demodulate and decode the narrowband signal from the downconverted received signal comprising an antenna, a switch filter, an amplifier, a mixer, a demodulator, an analog-to-digital converter (ADC), a baseband processor configured to decode a narrowband and wideband received signal, and a RF PLL as described above. The AAPA further discloses the receiver comprising an intermediate frequency phase lock loop (IF PLL) in electrical communication with the demodulator, the IF PLL being operative to generate the intermediate frequency oscillation signal (Fig. 1, element 36). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Lucidarme satisfies the limitations of the claim.

Regarding to Claim 24, the AAPA in view of Lucidarme discloses a wireless wideband receiver for downconverting a received signal having a wideband and narrowband signal components comprising a single downconverter path and a baseband processor in electrical communication with the downconverter being operative to demodulate and decode the narrowband signal from the downconverted received signal comprising an antenna, a switch filter, an amplifier, a mixer, a demodulator, an analog-to-digital converter (ADC), a baseband processor configured to decode a narrowband and wideband received signal, a RF PLL and an

IF PLL as described above. The AAPA further discloses the demodulator is a quadrature demodulator operative to demodulate the received signal into two demodulated signals having quadrature phase (Fig. 1, elements 34, 46, 38a/b & Specification, Page 8, lines 3-18). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Lucidarme satisfies the limitations of the claim.

Regarding to Claim 25, the AAPA in view of Lucidarme discloses a wireless wideband receiver for downconverting a received signal having a wideband and narrowband signal components comprising a single downconverter path and a baseband processor in electrical communication with the downconverter being operative to demodulate and decode the narrowband signal from the downconverted received signal comprising an antenna, a switch filter, an amplifier, a mixer, a demodulator, an analog-to-digital converter (ADC), a baseband processor configured to decode a narrowband and wideband received signal, a RF PLL and an IF PLL as described above. The AAPA further discloses the ADC comprising two ADC's operative to convert the two received signals to digital signals (Fig. 1, elements 42 a/b, 52 a/b). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Lucidarme satisfies the limitations of the claim.

Regarding to Claim 26, the AAPA in view of Lucidarme discloses a wireless wideband receiver for downconverting a received signal having a wideband and narrowband signal components comprising a single downconverter path and a

baseband processor in electrical communication with the downconverter being operative to demodulate and decode the narrowband signal from the downconverted received signal comprising an antenna, a switch filter, an amplifier, a mixer, a demodulator, an analog-to-digital converter (ADC), a baseband processor configured to decode a narrowband and wideband received signal, a RF PLL and an IF PLL as described above. The AAPA further discloses the narrowband channel having a bandwidth of 30kHz and the wideband channel have a bandwidth of 200kHz (Fig. 1, elements 26, 28, 54 & Specification, Page 7, lines 3-5, 15-21). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the AAPA in view of Lucidarme satisfies the limitations of the claim.

Response to Arguments

6. Applicant's arguments filed on September 27th, 2004 have been fully considered but they are not persuasive. The arguments presented that the AAPA does not teach implementing a single downconverter for downconverting both the wideband and narrowband signals of the received signal, however Fig. 1 elements 16-52 (Prior Art) represent a single downconverter that downconverts both a wideband and narrowband components and a baseband processor in electrical communication with the downconverter operative to decode the narrowband signal from the downconverted signal. The Specification (Paragraph 11) on Page 4, lines 20-25-to-Page 5, lines 1-5 describes that the downconverter **comprises** at least on ADC, a quadrature demodulator, a mixer, a RF oscillator,

a RF PLL and an amplifier, accordingly Fig. 1, elements 16-52 represent a single downconverter, thus the original rejection has been maintained.

7. Applicant's amendment further necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.**

See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (571)-272-3038. The examiner can normally be reached on M-F: 9am-6pm.
- If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571)-272-3056
 - The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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- Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sudhanshu C. Pathak



STEPHEN CHIN
SUPERVISORY PATENT EXAMINE
TECHNOLOGY CENTER 2800